In the Claims:

1. (Currently Amended) Connecting metalization for use in a[[A]] semiconductor device comprising:

a dielectric layer defining at least one aperture therein;

a barrier layer formed along the bottom and side walls of said at least one aperture;

a high temperature superconductor (HTS) layer formed over and coating the barrier layer in said at least one aperture; [[and]]

a tantalum layer in direct contact with and covering said HTS layer; and

a conductive material in direct contact with said tantalum layer and filling said aperture in said dielectric layer to form said connecting metalization.

2. (Original) The semiconductor device of claim 1 wherein the dielectric layer is a low-k dielectric material.

3. (Original) The semiconductor device of claim 1 wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.

4. (Cancel)

5. (Cancel)

6. (Original) The semiconductor device of claim 1 wherein the HTS material is a rare earth cuprate (copper oxide) material.

7. (Original) The semiconductor device of claim 1 wherein the HTS material is a rare earth element combined with barium copper oxide.

8. (Original) The semiconductor device of claim 7 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

9. (Original) The semiconductor device of claim 7 wherein the HTS material is yttrium barium copper oxide.

10. (Original) The semiconductor device of claim 1 wherein said HTS layer is a rare earth Ruthenium Oxocuprate.

11. (Original) The semiconductor device of claim 10 wherein said rare earth Ruthenium Oxocuprate is defined by the formula $RuSr_x$ (rare earth element) Cu_yO_z in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45, and z is between about 7.55 and 8.45.

12. (Original) The semiconductor device of claim 11 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

13. (Original) The semiconductor device of claim 1 wherein the HTS layer has a thickness of between 10 Å to 500 Å.

14. (Original) The semiconductor device of claim 1 wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.

15. (Original) The semiconductor device of claim 1 wherein the aperture defined in said dielectric has a width less than about 300 Å.

16. (Cancel)

17. (Original) The semiconductor device of claim 1 wherein said at least one aperture includes at least two trenches.

18. (Original) The semiconductor device of claim 17 wherein one of said at least two trenches further includes a via.

19. (Original) The semiconductor device of claim 1 further comprising a capping layer over said conductive metal filling said at least one aperture.

20. (Original) The semiconductor device of claim 19 wherein said capping layer is an HTS capping layer.

21. (Original) The semiconductor device of claim 19 further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.

22. (Original) The semiconductor device of claim 19 further including a hard mask over said HTS capping layer.

23. (Original) The semiconductor device of claim 22 wherein said hard mask is a layer of ARC.

24. (Original) The semiconductor device of claim 21 wherein said HTS capping layer has a thickness between about 10 Å and 500 Å.

25. (Currently Amended) Connecting metalization for use in a [[A]] semiconductor device comprising:

a first dielectric layer defining at least one aperture therein;

a barrier layer formed along the bottom and side walls of said at least one aperture;

a high temperature superconductor (HTS) layer formed over and coating said barrier layer;

a tantalum layer in direct contact with and covering said HTS layer;

a conductive material filling said at least one aperture in said first dielectric layer;

an HTS capping layer over said conductive material filling said at least one aperture; and

another dielectric layer over said first dielectric layer and said HTS capping layer.

26. (Original) The semiconductor device of claim 25 wherein said HTS capping layer has a thickness of between about 10 Å and 500 Å.

27. (Original) The semiconductor device of claim 25 wherein said aperture in said first dielectric layer has a width less than about 300 Å

28. (Original) The semiconductor device of claim 25 wherein the HTS material is a rare earth cuprate (copper oxide) material.

29. (Original) The semiconductor device of claim 25 wherein the HTS material is a rare earth element combined with barium copper oxide.

30. (Original) The semiconductor device of claim 29 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

31. (Original) The semiconductor device of claim 29 wherein the HTS material is yttrium barium copper oxide.

32.-56. (Cancel)

57. (New) Connecting metalization for use in a semiconductor device comprising:

a dielectric layer defining at least one aperture therein;

a barrier layer formed along the bottom and side walls of said at least one aperture;

a high temperature superconductor (HTS) layer formed over and coating the barrier layer in said at least one aperture; and

a conductive material in direct contact with said HTS layer and filling said aperture in said dielectric layer to form said connecting metalization.

58. (New) The semiconductor device of claim 57 wherein the dielectric layer is a low-k dielectric material.

59. (New) The semiconductor device of claim 57 wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.

60. (New) The semiconductor device of claim 57 wherein the HTS material is a rare earth cuprate (copper oxide) material.

61. (New) The semiconductor device of claim 57 wherein the HTS material is a rare earth element combined with barium copper oxide.

62. (New) The semiconductor device of claim 61 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

63. (New) The semiconductor device of claim 61 wherein the HTS material is yttrium barium copper oxide.

64. (New) The semiconductor device of claim 57 wherein said HTS layer is a rare earth Ruthenium Oxocuprate.

65. (New) The semiconductor device of claim 64 wherein said rare earth Ruthenium Oxocuprate is defined by the formula $RuSr_x$ (rare earth element) Cu_yO_z in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45, and z is between about 7.55 and 8.45.

66. (New) The semiconductor device of claim 65 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

67. (New) The semiconductor device of claim 57 wherein the HTS layer has a thickness of between 10 Å to 500 Å.

68. (New) The semiconductor device of claim 57 wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.

69. (New) The semiconductor device of claim 57 wherein the aperture defined in said dielectric has a width less than about 300 Å.

70. (New) The semiconductor device of claim 57 wherein said at least one aperture includes at least two trenches.

71. (New) The semiconductor device of claim 71 further comprising a capping layer over said conductive metal filling said at least one aperture.

72. (New) The semiconductor device of claim 71 wherein said capping layer is an HTS capping layer.

73. (New) The semiconductor device of claim 71 further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.

74. (New) The semiconductor device of claim 74 further including a hard mask over said HTS capping layer.

75. (New) The semiconductor device of claim 74 wherein said hard mask is a layer of ARC.

76. (New) Connecting metalization for use in a semiconductor device comprising:

a first dielectric layer defining at least one aperture therein;

a barrier layer formed along the bottom and side walls of said at least one aperture;

a high temperature superconductor (HTS) layer formed over and coating said barrier layer;

a conductive material in direct contact with said HTS layer and filling said at least one aperture in said first dielectric layer to form said connecting metalization;

an HTS capping layer over said conductive material filling said at least one aperture; and

another dielectric layer over said first dielectric layer and said HTS capping layer.

77. (New) The semiconductor device of claim 76 wherein the HTS material is a rare earth cuprate (copper oxide) material.

78. (New) The semiconductor device of claim 76 wherein the HTS material is a rare earth element combined with barium copper oxide.

79. (New) The semiconductor device of claim 78 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

80. (New) The semiconductor device of claim 29 wherein the HTS material is yttrium barium copper oxide.